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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

DIGITAL DESIGN & COMPUTER ORGANISATION

CCA-1

TITLE : DIGITAL LOCK SYSTEM

BATCH NO: 20

SEM : 3rd SEM

SECTION : CSE-12

DATE OF SUBMISSION: 17/12/2025

SUBJECT CODE: BCS302

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ABSTRACT

This project focuses on the design and implementation of a digital lock system that operates using a predefined 4-bit password. The objective is to combine both combinational and sequential digital logic to build a reliable and efficient locking mechanism. The core functionality is achieved using basic logic gates such as AND and NOT to verify whether the entered password matches the stored access code. Once the correct combination is detected, the output of the combinational circuit generates a high signal, which is then captured and held by a D flip-flop on the rising edge of the clock. This use of a flip-flop ensures that the unlock signal remains stable and synchronized with the clock, thus demonstrating sequential circuit behaviour.

The entire design is modelled using VHDL, enabling precise hardware description and simulation. The simulation waveforms validate the correctness of the logic implementation and confirm that the lock responds appropriately to both valid and invalid password inputs. Through this experiment, students gain practical exposure to digital circuit design, logic gate-level implementation, flip-flop operation, and HDL-based verification. This digital lock system represents a fundamental application of digital design principles commonly used in security systems, embedded devices, and access control applications.

INTRODUCTION

Digital systems form the basis of many modern electronic applications, especially in areas related to security and access control. One such application is a digital lock, which grants access only when a correct password is entered. This experiment focuses on designing a simple digital lock using a 4-bit password, logic gates, and a flip-flop to demonstrate the integration of combinational and sequential digital circuits.

The password entered by the user is compared with a predefined code using basic logic gates such as AND and NOT. This comparison produces a high output only when all bits of the password match exactly, representing the combinational part of the system. To ensure that the unlock signal is stable and synchronized with the system clock, a D flip-flop is used to store the comparison result. This introduces the sequential aspect of the design, where the output changes only on the rising edge of the clock.

The entire design is implemented using VHDL, allowing accurate modeling and simulation of the circuit's behaviour. Simulation results verify that the lock activates only for the correct password, while all incorrect combinations prevent access. Through this experiment, students gain practical understanding of logic gate design, flip-flop operation, and hardware description language usage.

DESIGN

TRUTH TABLE

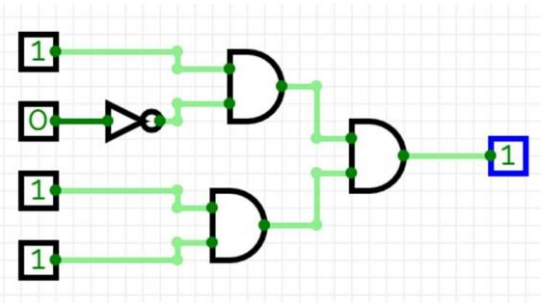
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

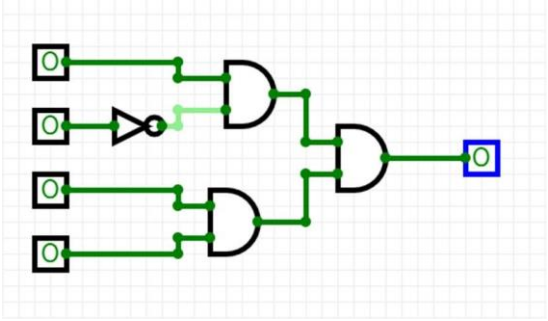
K-MAP SIMPLICATION

AB\CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	1	0

Equation: Y=AB’CD

Circuit Diagram:



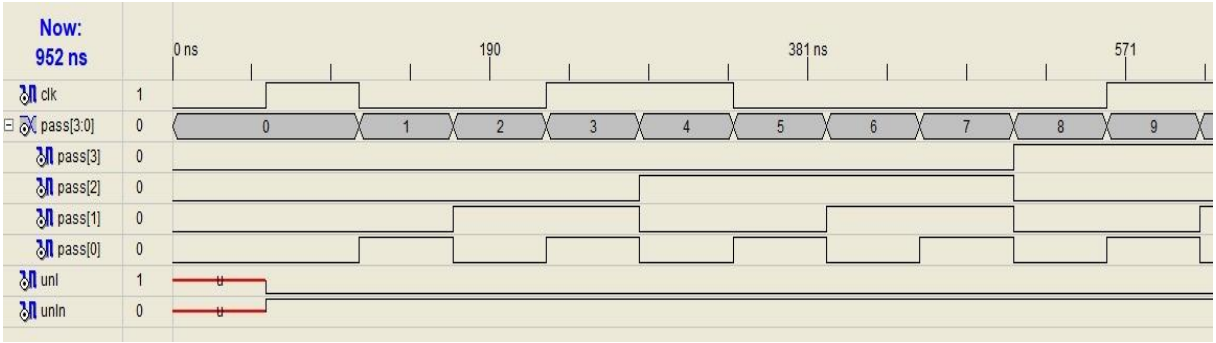


CODE (VHDL)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity fbhcgfxghy is
    Port (
        clk  : in  STD_LOGIC;
        pass : in  STD_LOGIC_VECTOR (3 downto 0);
        unl  : out STD_LOGIC;
        unln : out STD_LOGIC
    );
end fbhcgfxghy;
architecture Behavioral of fbhcgfxghy is
    signal d : STD_LOGIC;
    signal q : STD_LOGIC;
```

```
begin
    -- Password check: 1011
    d <= pass(3) and (not pass(2)) and pass(1) and pass(0);
    process(clk)
    begin
        if rising_edge(clk) then
            q <= d;
        end if;
    end process;
    unl  <= q;
    unln <= not q;
end Behavioral;
```

TESTBENCH



APPLICATION

Electronic Door Locks

Digital locks are commonly used in homes, offices, and secure facilities where access is granted only after entering the correct password.

Security Safes and Lockers

Many electronic safes use similar password-based locking mechanisms to protect valuable items and confidential documents.

Access Control Systems

Password-based entry systems are widely used in laboratories, server rooms, and restricted zones to ensure authorized access.

Embedded Systems and IoT Devices

Microcontroller-based systems often incorporate digital lock circuits for user authentication and system protection.

Consumer Electronics

Devices such as digital cabinets, electronic toys, and password-protected storage boxes use basic digital lock logic.

Educational and Training Applications

The design is useful for teaching combinational and sequential circuit design, logic gate implementation, and VHDL programming in academic labs.

CONCLUSION

The design and implementation of the digital lock system successfully demonstrate the fundamental principles of digital logic and hardwarebased security mechanisms. By integrating combinational logic with sequential elements, the project illustrates how real-world digital systems authenticate user inputs and generate controlled outputs. The 4-bit password verification was achieved using basic logic gates, where the predefined password was translated into a Boolean expression and simplified for implementation. The resulting logic accurately identifies the correct password by evaluating each bit through AND and NOT operations.

To ensure reliable and stable system behavior, the output of the combinational logic was stored in a D flip-flop, enabling synchronization with the rising edge of the clock signal. This sequential component prevents glitches, ensures predictability, and provides a clean unlock signal that remains valid until the next clock event. The use of VHDL further enhanced the design process by allowing behavioral and structural modeling, simulation, and verification of the circuit before hardware implementation. Simulation waveforms confirmed that the output is activated exclusively for the correct password combination, validating the effectiveness of both the logic design and the VHDL implementation.

Overall, this experiment provides valuable experience in designing secure digital systems, applying Boolean algebra, constructing logic circuits, and understanding the role of flip-flops in digital storage. It also highlights the practical importance of hardware description languages in modern digital design workflows. The successful realization of the digital lock system reinforces key concepts in digital electronics and demonstrates how these principles are used in real-world applications such as access control, embedded systems, and automated security devices.

REFERENCE

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